four parallel capacitor plates is arranged opposite a next said respective plurality of vias, with identical spacing of vias in each plurality of vias.

A marked up copy of claim 1, showing all changes made relative to the previous version of the claim, accompanies this paper on a separate sheet or sheets per 37 CFR § 1.121(c)(1)(ii).

REMARKS

Claims 1-12 are pending in the application. Claim 1 is amended and new claim 12 is added. No new matter is added. Support for the features added to claim 1 (each of the at least four line pairs of the at least four parallel capacitor plates is connected by a plurality of vias, i.e., by more than one via) and by claim 12 (essentially, that the plurality of vias in each line pair is spaced identically as in each next line pair so that the vias of the various line pairs are arranged opposite one another), can be found in Figs. 2B and 2C, and in the accompanying description in the specification, for example Page 5, line 10 through page 7, line 17.

Regarding some of the comments made in the final Office action mailed on Aug. 9, 2001, applicants respond as follows.

The final Office action asserts that reference characters 27 and 30 have both been used to designate conductive via and dielectric layer. Applicants respectfully submit that label 27 correctly indicates a second dielectric layer (page 5, lines 3-4;

Figs. 2B and 2C). Label 27 uses an arrow, which represents that the entire layer is being indicated. Labels 30 correctly point directly to individual vias 30 of the plurality of vias that are formed in and pass through the dielectric layer 27 to connect the line pair of conductive lines 22 and 23 (page 5, lines 11-14).

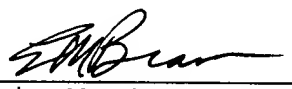
The final Office action asserts that Fig. 2B depicts a dielectric layer comprising vacuum. Applicants respectfully submit that the disclosure does not describe vacuum, but rather the claims recite (and the disclosure supports) dielectric layers 27-29 (e.g., page 5, line 13). Only claim 4 recites that the dielectric layers must comprise silicon oxide. In any case, the dielectric layers 27-29 are clearly indicated in the drawing figures.

The final Office action rejects claims 1-11 under 35 U.S.C. § 103(a) over U.S. Patent No. 5,583,359 to Ng et al. Applicants respectfully traverse this rejection. Independent claim 1, from which claims 2-12 depend, recite that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective plurality of vias. Ng et al. do not teach or suggest this patentable feature. Conversely, the apparatus of Ng et al. has the line pairs connected by a single via only (for example, line pair 210,212 is connected only by via 240 (figs. 8 and 9). This is not mere design choice because applicants discovered that using multiple via connections between line pairs (claim 1) with identical spacings (claim 12) improves the capacitor

effect. Accordingly, since these features are not found in the cited references, withdrawal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

In view of the foregoing, applicant respectfully requests that the Examiner withdraw the rejections of record, allow all the pending claims, and find the present application to be in condition for allowance. If any points remain in issue that the Examiner feels may best be resolved through a personal or telephonic interview, he is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Eric M. Bram, Reg. 37,285
Attorney for Applicant(s)

U.S. Philips Corp.
580 White Plains Road
Tarrytown, NY 10591
(914) 333-9635

Marked-up version of amended claims to show changes made:

1. (Twice Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane,

each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

~~a plurality~~ an array of vias arranged such that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective ~~one of the~~ plurality of vias, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.